



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,526	04/26/2006	Leah M. P. Pastel	BUR920030080US1	2272
33074 7590 06/30/2009 INTERNATIONAL BUSINESS MACHINES CORPORATION DEPT. 18G BLDG. 321-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533				
EXAMINER VELEZ, ROBERTO				
ART UNIT 2829		PAPER NUMBER		
NOTIFICATION DATE 06/30/2009		DELIVERY MODE ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

EFIPLAW@US.IBM.COM

**Continuation Sheet**

1. Applicant argues that the term "bus" as used in the present application differs from the term "bus" used by Teene, and that this difference needs to be recognized. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., quiescent voltage bus is a quiescent power distribution grid within the IC, separate from the global voltage bus) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
2. Applicant argues that the power supply bus 16 and the internal power bus 14 in Teene perform the same function. The Examiner respectfully disagrees. The function of the power supply bus 16 is to provide power to the internal power bus 14, and the function of internal power bus 14 is to provide power to the gate array cells, as disclosed by Teene. Therefore, even though both the power supply bus 16 and the internal power bus 14 provide power, different functionalities are performed.
3. Applicant argues that adding Sagasawara to the combination of Teene and Jennion teaches away from the Applicants who teach a global power grid, a quiescent power grid, and header switches that can be used to select which functional circuits load the power grids. The Examiner respectfully disagrees. Sagasawara is related to performing a tester based IDDQ current measurement, similar to what the combination of Teene and Jennion are related to. Therefore, the combination of Sagasawara, Teene and Jennion is obvious and does not teach away.

4. Applicant argues that Teene, Jennion and Sagasawara in combination are not compatible implementations, because it would be difficult to implement any of the stated teachings on the same IC circuitry. In response to applicant's argument that the combination of Teene, Jennion and Sagasawara are not compatible implementations, the test for obviousness is not whether the features of secondary references may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

/Ha T. Nguyen/

Supervisory Patent Examiner, Art Unit 2829